IN THE CLAIMS:

This listing of the claims will replace all prior versions, and listing, of claims in the application or previous response to office action:

1. **(Currently Amended)** A synchronization method for a reception unit, said method comprising:

transmitting synchronization signals from a transmission unit to at least one reception unit;

supplying said synchronization signals ~~from said at least one reception unit~~ to a ~~first clock transmitter~~phase locked loop (PLL) unit having a phase regulator, said ~~first clock transmitter~~PLL unit generating ~~outputting~~ a first clock signal comprising a stable number of clock signals between two of said synchronization signals; and

if said PLL unit does not operate stable then controlling

~~driving~~ a ~~second~~ controllable clock ~~transmitter~~ generation unit ~~using~~ with a predetermined control signal for generating a second clock signal, and

if said PLL unit operates in a stable mode then ~~said stable clock signals, said~~ controlling said ~~second~~ clock ~~transmitter~~ generation unit ~~ng~~ ~~a second clock signal which is continuously present~~with a signal generated by said phase regulator to generate said second clock signal and comparing ~~, even when said stable clock signals are absent, wherein~~ a phase difference arising between said first clock ~~transmitter~~ signal and said second clock ~~transmitter~~ signal ~~is compensated for by influencing a period duration of~~ to generate a compensation signal for said ~~second~~ clock ~~transmitter~~generation unit, wherein said ~~period duration of said second clock transmitter is influenced such that a shorter interval between phases of said stable clock signals and said second clock signal are reduced~~compensation signal reduces the phase difference with predetermined steps.

2. **(Currently Amended)** The method of claim 1, wherein only slight changes in said ~~period duration~~output clock signal ~~of said second clock transmitter~~ are made by said compensation signal such that said phase difference is continuously reduced within a prescribed time period until said ~~stable~~ first clock signals and said second clock signal are synchronous with one another.

3. (Cancelled)

4. **(Cancelled)**

5. **(Cancelled)**

6. **(Currently Amended)** The method of claim 5, wherein corrections in ~~said~~ a period duration of said first clock ~~transmitter~~signal, which are ascertained by said phase regulator from clock pulse to clock pulse, are taken into account both in said ~~stable~~ first clock signal and in said second clock signal.

7. **(Currently Amended)** A reception unit for synchronizing signals, said reception unit comprising:

a first clock transmitter, said first clock transmitter comprising a phase locked loop (PLL) unit outputting a first clock signal comprising a stable number of clock signals between two of synchronization signals received from a transmission unit; and

a second clock transmitter, said second clock transmitter using said ~~stable~~ first clock signals, said second clock transmitter generating a second clock signal ~~which is continuously present, even~~with a predetermined clock frequency when said ~~stable~~ first clock signals are absent, and generating said second clock signal by means of an output signal of a phase regulator in said PLL unit, wherein a phase difference arising between said first clock ~~transmitter~~ signal and said second clock ~~transmitter~~ signal is compensated for by ~~influencing a period duration of~~ controlling said second clock ~~transmitter~~signal in such a way that the phase difference between the first and second clock signal is reduced with predetermined steps~~, wherein fluctuations in said period duration of said first clock transmitter, which are corrected by said phase regulator, are mapped onto said second clock transmitter~~.

8. **(Currently Amended)** The method of claim 7, wherein said phase regulator, upon receiving said synchronization signals, ascertains instantaneous phase errors and readjusts said first clock ~~transmitter~~ signal such that said first clock transmitter outputs a nominal number of clock signals between two synchronization signals.

9. (Cancelled)

10. **(NEW)** A circuit for synchronizing signals comprising:

- a phase locked loop (PLL) circuit receiving synchronization signals and generating a first clock signal comprising a predetermined number of clock pulses between subsequent synchronization signals, wherein the PLL circuit comprises a phase regulator generating a phase regulating signal;

- a clock generation circuit receiving a control signal for generating a second clock signal,

- a phase comparator for comparing the phases of said first clock signal and said second clock signal, wherein said phase comparator generates a phase comparison signal;

- a control unit for generating said control signal, wherein said control unit receives said phase regulating signal and wherein said control signal generates an independent control signal to generate said second clock signal in case said PLL circuit operates in an unlocked mode and provides said phase regulating signal to said clock generation circuit in case said PLL circuit operates in a locked mode, wherein said control unit receives said phase comparison signal and adjusts said second clock signal stepwise to compensate a phase difference between said first and second clock signal.

11. **(NEW)** The circuit according to claim 10, wherein steps in said stepwise adjustment of said phase are small in comparison to said phase difference.

12. **(NEW)** The circuit according to claim 10, wherein said clock generation circuit comprises a controllable clock generator followed by a frequency divider.

13. **(NEW)** The circuit according to claim 12, wherein said frequency divider is followed by a clock counter, wherein said clock counter generates said second clock signal.

14. **(NEW)** The circuit according to claim 10, wherein said PLL circuit comprises a controllable clock generator followed by a frequency divider followed by said phase regulator.

15. **(NEW)** The circuit according to claim 14, wherein said frequency divider is followed by a clock counter, wherein said clock counter generates said first clock signal.